SGS-THOMSON MICROELECTRONICS

CB22000 SERIES

HCMOS STANDARD CELL

FEATURES

- 0.7 micron, double layer metal HCMOS4T process featuring self-aligned twin tub N and P wells, low resistance polysilicide gates and thin metal oxide.
- 2 - input NAND (ND2P) delay of 0.30 ns (typ) with fanout = 2.
- True not pseudo TTL output buffers.
- Output buffers capable of driving ISA, EISA, MCA, and SCSI interface levels.
- Broad range of 230 periphery and core cells.
- 180 element macrofunction library.
- Module generators to support megacells.
- Maximum gross gate count of 170,000.
- Nominal density of 1250 gates/mm^2.
- Fully independent power and ground configurations for core and I/O cells.
- High drive I/O capability of sinking up to 24 mA with slew rate control and current spike suppression.
- Flexible 5 V and 3.3 V **(1)** power supply choice.
- Active pull up and pull down devices.
- Buskeeper functions.**(1)**
- Design For Test includes LSSD macro library option for megacells and IEEE 1149.1 JTAG Boundary Scan architecture.
- Cadence based design system with interfaces from multiple workstations.
- Broad ceramic and plastic package range.
- Latchup trigger current > + / - 500 mA.
- ESD protection > + / - 4000 volts.

GENERAL DESCRIPTION

The CB22000 STANDARD CELL series uses a high performance, double level metal HCMOS process to achieve sub-nanosecond internal speeds, while at the same time, offering low power dissipation and high noise margin. The maximum equivalent gate count is 170,000. Even higher effective utilizations are achieved with the optimization of megacells, for single port RAM, dual port RAM multiplier and ROM.

The output buffers have drive strengths capable of sinking up to 24 mA and sourcing up to 12 mA without limiting the functionality of adjoining cells. Output buffers are electrically compatible with EISA, ISA, MCA and SCSI interface standards. The CB22000 Series is compatible with the successful ISB24000 Series for design transfer from Continuous Array to Standard Cell for high volume production. The CB22000 will support a 3.3 V power supply option and allow the core and I/O to be powered from different voltage levels for an optimal combination of performance, power consumption and interface compatibility. Testability is supported at device level with the close coupling of the scan path flip flops, automatic test pattern generation and high pattern depth tester architectures. At the system level testability, IEEE 1149.1 JTAG is fully supported within the I/O of each array.

A wide range of CAD tools are combined into the design system allowing design development on a choice of workstations. An extensive package offering makes this series well suited for a broad range of high performance applications. The product technology may be used in commercial, industrial and military environments.

MODULE GENERATORS

SPRAM Generator	DPRAM Generator	Multiplier Generator	ROM Generator
Fully static, synchronous operation	Fully static, synchronous operation	Signed two's compliment	Fully static, synchronous operation
80 Kbits max capacity	64 Kbits max capacity	6 to 64 Multiplicand bits	64 Kbits max capacity
8 to 16K Words -1 to 80 bits	16 to 8K Words - 1 to 80 bits	6 to 64 Multiplier bits	32 to 8K Words 1 to 32 bits
Multiplex Factor - 2, 4, 8, 16, 32	Multiplex Factor - 2, 4, 8, 16	12 to 128 Product bits	Multiplex factor - 8, 16, 32

Note: 1. Please consult your local SGS-THOMSON Sales Office for latest information.

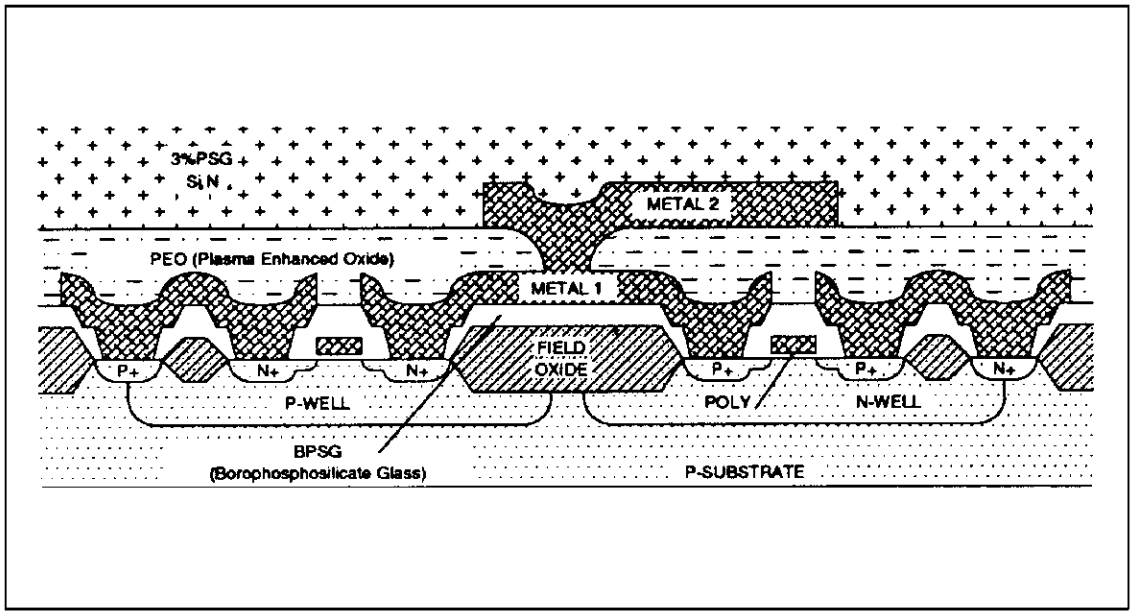
TECHNOLOGY OVERVIEW

The CB22000 series STANDARD CELL architecture, as previously used with the CB12000 series is a horizontal series of cells with interconnections between each row. Each row has a set of feedthroughs routing in the vertical direction. Surrounding the core are the I/O cells and V_{DD}/V_{SS} pads. Two levels of metal are used. Metal 1 is used for power distribution and cell to cell wiring in the horizontal direction. Metal 2 is used for power distribution and cell to cell connections in the vertical direction. Metal 1 is also used for intracell wiring.

Cell height and grid size have been optimised and the compact geometry of the transistors assure a density of 1100 gates/mm^2 for core logic and 1350 gates/mm^2 for generators. Optimum performance is offered through width/length sizing methodology which uses cell internal stepdowns for minimum input capacitance.

Power distribution for the complete device consists of a set of 6 power and ground rings which surround the core logic. In addition, power is supplied to the core cells by means of two single V_{DDint}/V_{SSint} and V_{DDext}/V_{SSext} respectively.

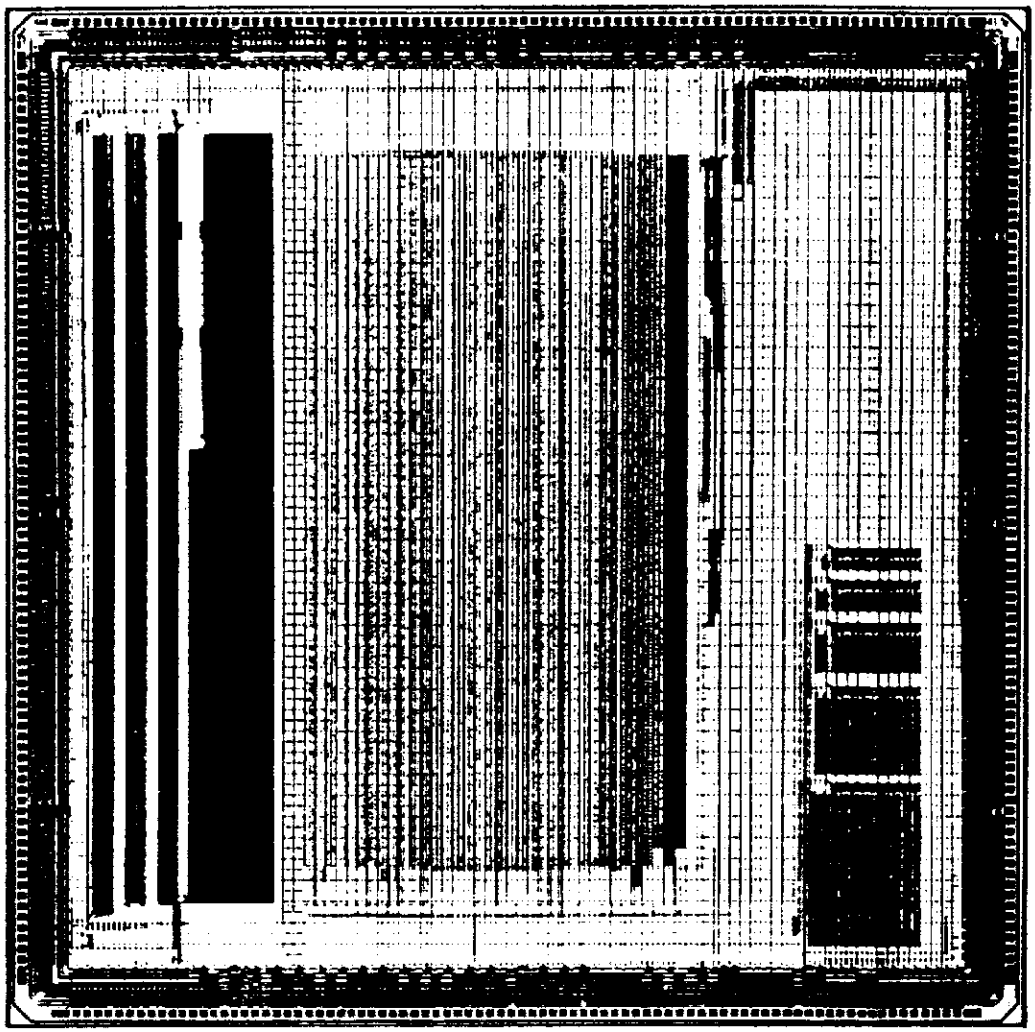
Figure 1. Double Level Metal Architecture



EVALUATION DEVICE

An evaluation device is available to demonstrate the performance of the CB22000 series as well as verify the effectiveness of the design system. The device has path delays, latches and a host of macrocells which were used to verify the simulated characteristics that are supplied in the data book. Characterization of the path delays shows typical delays of 300 ps for a 2 input NAND with receivers/drivers operating at frequencies in excess of 100 MHz. The evaluation device is available in a 120 pin CPGA package.

Figure 2. Evaluation Device



LIBRARY

The following section details the elements which make up the CB22000 Series library. The elements are organized into three categories

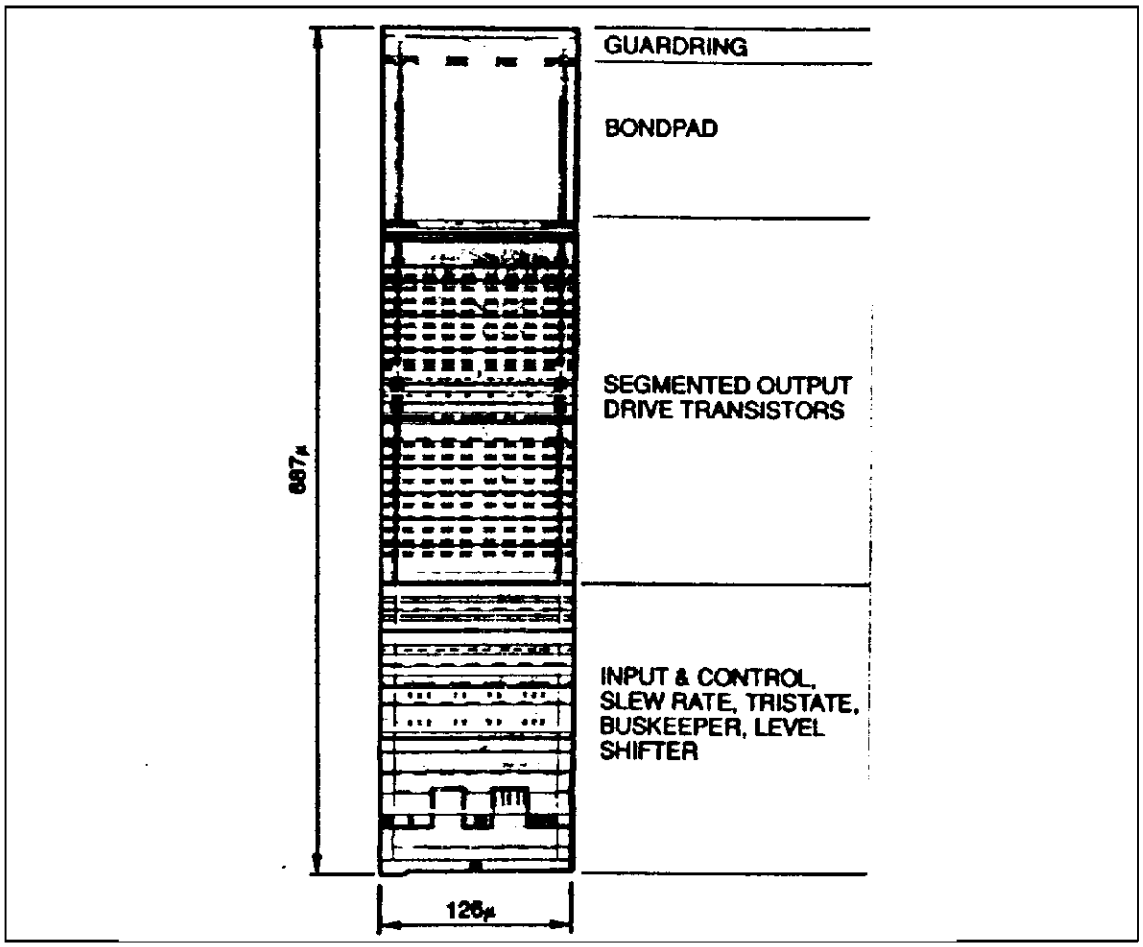
1. Macrocell library which includes Input, Output, Bidirectional Buffers and Core cells including JTAG macrocells.
2. Macrofunctions
3. Module Generators

I/O Buffers

The I/O buffers are located on the periphery of the array. Figure 3 is a plot of an I/O buffer. The basic cell consists of a bond pad with an input protection, an output driver section, and a receiver/pre-driver section. High impedance pull-up or pull-down resistors are also available in the I/O cell resistors. Input and output macrocells do not invert logic signals. The output transistors are provided with an independent power distribution metalization thereby minimizing switching transients in the periphery from affecting either the on chip receivers or the internal matrix.

Several important features are incorporated in the output drivers. These include slew rate control and current spike suppression. Slew rate is controlled by turning on individual sections of the large output transistor in a controlled manner. During normal switching a large surge of current occurs when a conventional CMOS buffer has both P and N channel transistors in conduction. This situation is avoided by placing the buffer in tri-state for approximately 200 ps during the time the buffer changes state. Each output buffer may be configured for up to 24 mA sink current (12 mA source)drive capability.

Figure 3. Full Function I/O Cell



True TTL Compatibility - The TTL bus driver buffers are designed to operate in conjunction with bipolar products on a common data bus. The output voltage swings and current drive capabilities are the same as bipolar TTL buffers. This allows the system designer to take advantage of the low power consumption of the CB22000 array CMOS logic while avoiding the problems with pseudo TTL buffers. Most CMOS array TTL buffers are standard CMOS buffers characterized at TTL levels and display various undesired operational nets to the 5 V rail due to their low impedance PMOS transistors. This slows down the net by increasing the discharge time and damages the bipolar TTL receivers connected to the net. The CB22000 buffers overcome this problem by not pulling to rail but switching to a maximum level of 4.1 V maximum as shown in Figure 4. Another problem associated with pseudo TTL buffers is the high input impedance exhibited when in tri-state mode. This can cause undesired reflections on the data bus and is overcome in the CB22000 by means of two diodes which exhibit input characteristics common to bipolar devices in tristate mode.

Standard Bus Compatibility - A subset of the TTL buffers conform to ISA, EISA, MCA and SCSI bus operating specifications. These buffers comply fully with the specification rise and fall times. Figure 4 and 5 show the D.C Specifications for True TTL Output Buffers and Input Receivers respectively. They target the high performance 32 bit RISC and CISC architectures and data communication systems. Selection of the correct output buffer is very important to achieve the desired performance.
Two parameters used to select the appropriate

Figure 4 D.C Specifications for True TTL Output Buffers

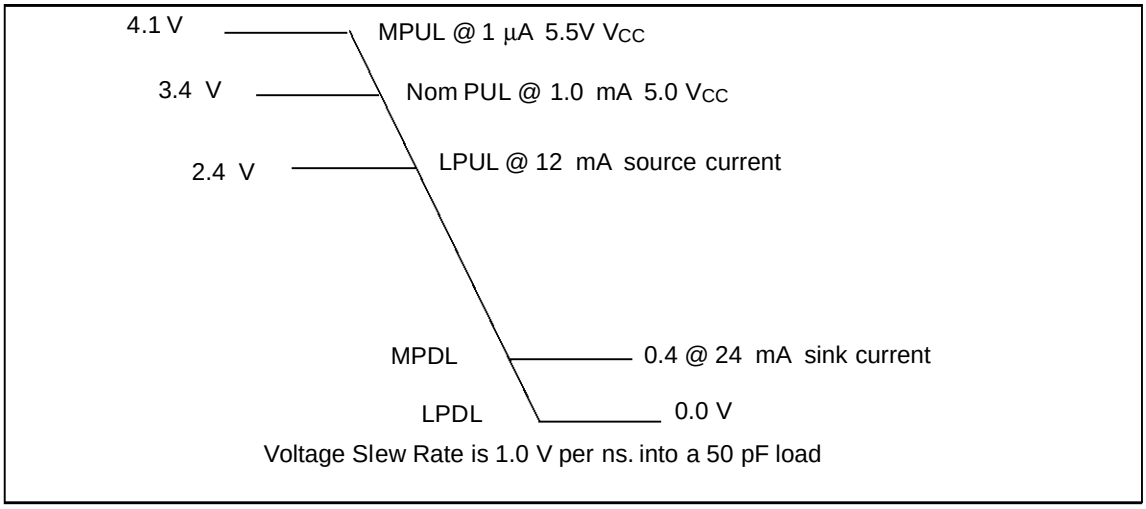
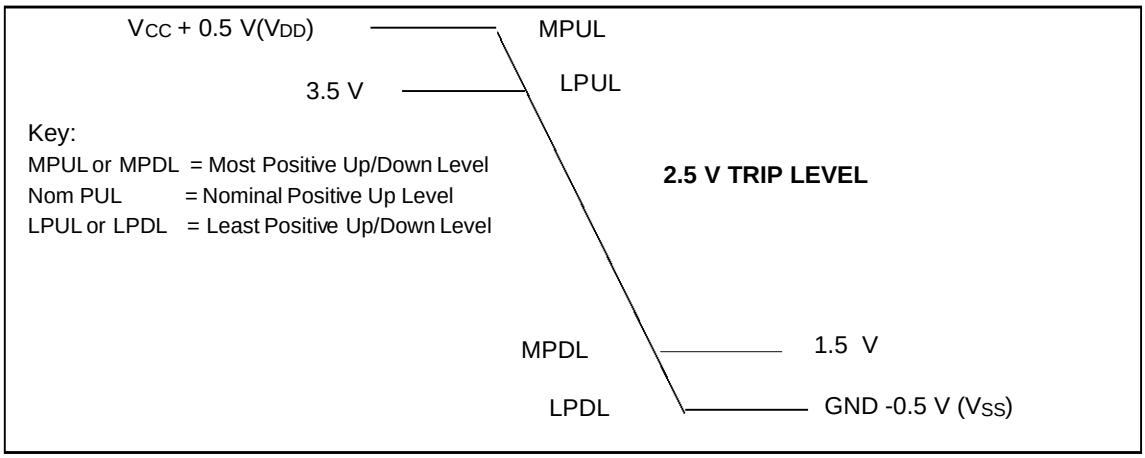


Figure 5 D.C Specifications for Input Receivers



buffer are maximum drive current and load capacitance, see Tables 1 and 2. Exceeding the maximum load capacitance will result in slower switching performance. Exceeding the maximum current may result in degraded levels of reliability. Standard CMOS and TTL levels are specified for all external buffer and Schmitt Trigger input receivers are also available. All buffers are designed for commercial, industrial and military operation.

Core Logic

Table 1. I/O Drive capability for slew rate control buffers

Current Drive (mA)	Standard Unit	Maximum Capacitance (pF)
4.0	2.0	100
8.0	4.0	200
12.0	6.0	300
16.0	8.0	500
24.0	12.0	750

Table 2. I/O Drive capability for non-slew rate control buffers

Current Drive (mA)	Standard Unit	Maximum Capacitance (pF)
4.0	4.0	100
8.0	8.0	200
16.0	16.0	500
24.0	24.0	750

Table 3. Temperature and Voltage Multipliers

Temperature (°C)	K_T
–55	0.74
–40	0.80
0	0.92
25	1.00
70	1.14
85	1.20
125	1.32

V_{DD} (V)	K_V
4.50	1.09
4.75	1.04
5.00	1.00
5.25	0.96
5.50	0.93

The propagation delays shown in the CB22000 data book and in the AC Characteristics section of this data sheet are given for nominal processing, 5V operation, and 25°C temperature conditions. However there are additional factors that affect the delay characteristics of the macrocells. These include loading due to fanout and interconnect routing, voltage supply, junction temperature of the device, processing tolerance and input signal transition time. Prior to physical layout, the design system can estimate the delays associated with any critical path. The impact of the placement and routing can be back annotated from the layout for final simulations of critical timing. The effects of junction temperature, (K_T) and voltage supply, (K_V) on the delay numbers are summarized in Table 3. A third factor, is associated with process variation. This multiplier has a minimum of 0.6 and a maximum of 1.6.

Macrocells And Macrofunctions

The CB22000 series has internal macrocells that are robust in variety and performance. Specialized cells for scan techniques and a mix of complex logic functions round off the SSI offering. High drive, double output power versions, which may be used to speed up critical paths, are available for most internal macrocells. Table 4 lists the macrocells available in the CB22000 library.

Macrofunctions are a series of soft-macros facilitating quick capture of large functional blocks and are available for such functions as counters, shift registers and adders. Macrofunctions are implemented at layout by utilizing macrocells and interconnecting to create the logic function.

Module Generators

A series of module generators are available to support a range of megacells. These modules enable the designer to choose individual parameters in order to create a compiled cell which meets the specific application requirements. The compiled cells are implemented using a special leaf cell technique which ensures predictable layout and accurate module characteristics.

Table 5 shows the characteristics of the generators available for single port RAM, dual port RAM, ROM and multiplier. In choosing megacells the designer can consider the trade-offs between speed and area to generate a fully customized cell which meets their specific device requirements.

Table 4. Macrocell Library Summary

Function	Total
Single Drive Gates and Inverters	34
Double Drive Gates and Inverters	26
Boolean Gates	13
Internal Tristate Buffers, Single/Double Drive	4
Flip Flops, Latches and RAM1, Single Drive	15
Latches with Scan Inputs	5
Flip Flops and Latches, Single Drive	7
Flip Flops and Latches, Double Drive	11
Full Adder	1
Multiplexers, MSI, Power Multiplexers	10
CORE CELL TOTAL	**126**
Input	16
Output	34
Bidirectional	39
Buskeeper	19
I/O BUFFER TOTAL	**108**
OVERALL TOTAL	**234**

Table 5. Module Generator Library

Cell	Description
SPRAM	1 port RAM (separate data I/O) - Synchronous - Capacity 80 Kbits max. 8 to 16 Kwords x 1 to 80 bits (mux= 2, 4, 8, 16, 32) AC Characteristics: Read Access Time 4.6 ns typical (1024 Words x 16 bits) Density:2700 bits/mm^2 (1k x 16)
DPRAM	2 port RAM (separate data I/O) - Asynchronous - Capacity 64 Kbits max. 16 to 8Kwords x 1 to 80 bits (mux = 2, 4, 8, 16) AC Characteristics: Read Access Time 15 ns typical (8192 Words x 8 bits) Density :1950 bits/mm^2 (1k x 16)
MULT	Signed two's compliment, dynamic multiplicand bits: 6 to 64 multiplier bits: 6 to 64 product bits: 12 to 128 AC Characteristics: Propagation Delay 46.5 ns (32 bits x 32 bits)
ROM	Synchronous, Capacity 64 Kbits 32 to 8K words x 1 to 32 bits (mux = 8, 16, 32) AC Characteristics: Read Access Time 24ns w.c. (2048 Words x 8 bits) Density: 23000 bits/mm^2 (1Kw x 8 bits)

DESIGN FOR TESTABILITY

The time and cost for ASIC testing increases exponentially as the complexity and size of the ASIC grows. Using a design for testability methodology allows large, more complex ASICs to be efficiently and economically tested.

CB22000 supports the JTAG boundary Scan and edge level sensitive design scan by providing the necessary macrocells. Scan testing aids device testability by permitting access to internal nodes without requiring a separate external connection for each node accessed. Testability is assured at device level with the close coupling of LSSD latch elements, Automatic Test Pattern Generation (ATPG) and high pattern depth tester architecture.

At system level, SGS-THOMSON fully supports IEEE 1149.1, within the array of each cell array member. Two types of scan cells are provided by the CB22000 Series library. They are FDxS/FJKxS cells which are edge sensitive and LSxx cells which are truly LSSD cells.

PACKAGE AVAILABILITY

The CB22000 Series is designed to be especially suitable for high volume surface mount applications, from 28 pin plastic leaded chip carriers (PLCC) up to 160 pin metric quad flatpacks (MQFP) with over 300 pin MQFPs in development. Pin counts for through board mounting range up to 299. For higher pin counts the range is compatible with the industry standard JEDEC and EIA-J Guardring Quad Flatpack (GQFP) with pin counts from 186 to 304.

The diversity in pin count and package style gives the designer the opportunity to find the best compromise for system size, cost and performance requirements.

All packages for the military market are hermetically sealed to meet MIL-STD-883 Method. Prototypes are developed in ceramic packages for fast turnaround evaluation.

DESIGN ENVIRONMENT

Several interface levels are possible between SGS-THOMSON and the customer in the undertaking of an ASIC design. The four levels of interface are shown in Figure 7. Level 1 is characterized by SGS-THOMSON receiving the system specification and taking the design through to validation and fabrication. At Level 2 interface the designer supplies a complete logic design implemented in a standard generic logic family. SGS-THOMSON then takes the design through to layout, validation and fabrication.

Level 3 is the most common and preferred interface level. Logic capture and pre-layout simulation are performed by the designer using a SGS-THOMSON supported design kit. The design is then taken through layout, validation and fabrication by SGS-THOMSON

The SGS-THOMSON design system validates all designs before fabrication. Design kits are provided that allow schematic entry via Mentor Graphics, Cadence and Valid Logic. Simulation is supported on Cadence and Mentor Graphics. Full support is also provided for Cadence Verilog, VHDL-XL and System Hilo simulators.
Figure 8 shows the SGS-THOMSON Design Flow.

New features of ASIC design include high level design methodology for circuit specification, verification and implementation. SGS-THOMSON supports the Synopsys Design Analyzer, Design Compiler and Test Compiler modules.

Figure 7. Customer SGS-THOMSON Interface Level

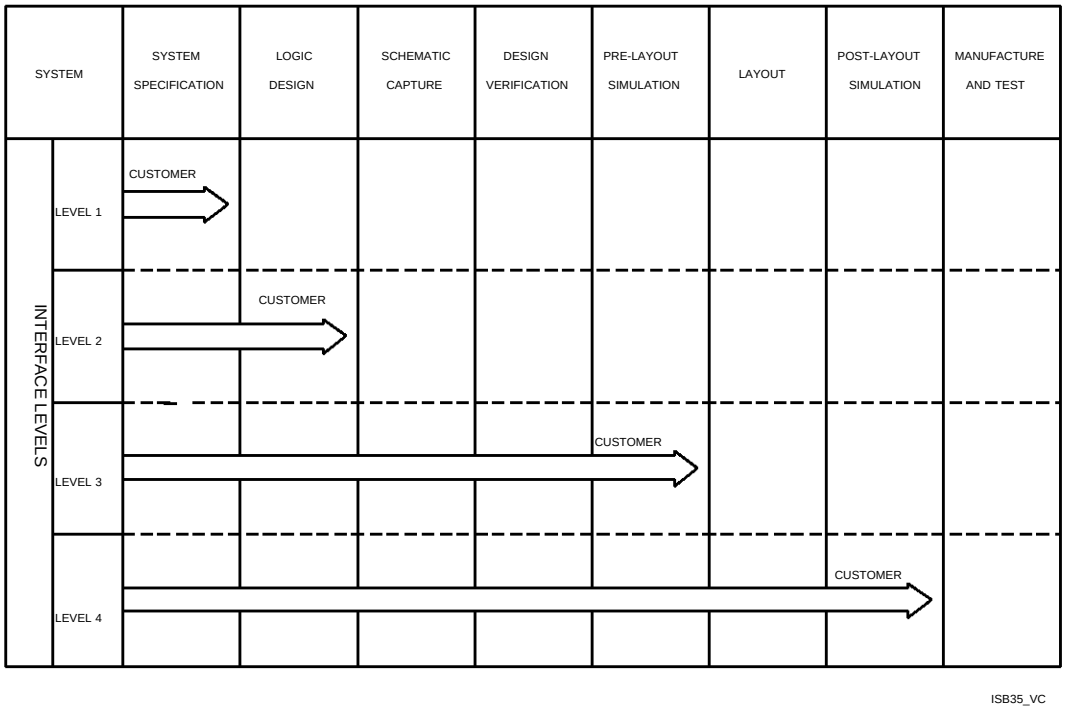
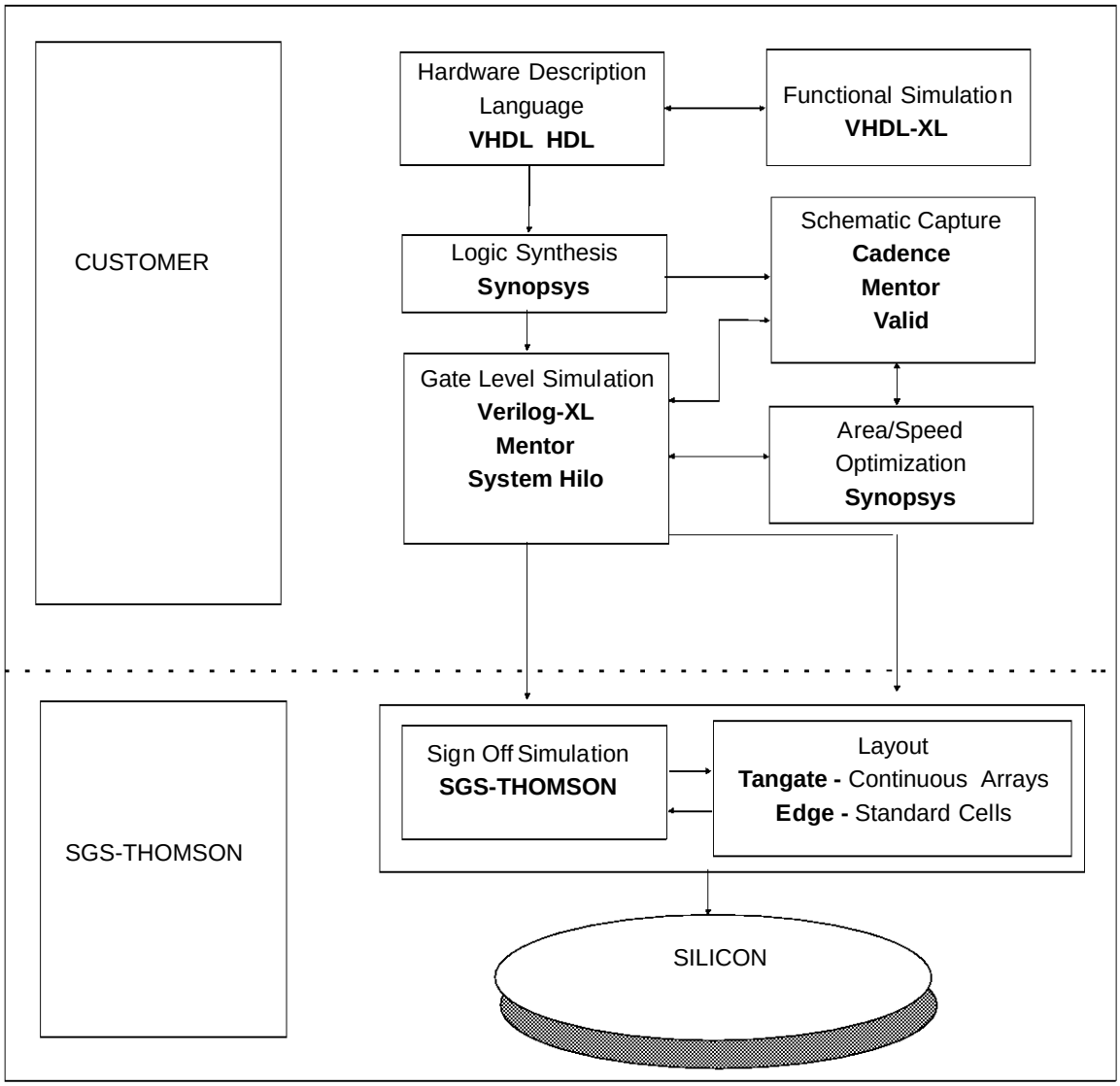


Figure 8. SGS-THOMSON Design Flow



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{DD}	– 0.50 V to + 7.00 V
Input or Output Voltage	– 0.50 V to (V_{DD} + 0.50) V
DC Forward Bias Current, Input Or Output	–12 mA (source) + 24mA (sink)
Storage Temperature (Ceramic)	– 65 to 150°C
Storage Temperature (Plastic)	– 40 to 125°C

Note 1: Referenced to V_{SS}. Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Operating Supply Voltage, V_{DD} – Commercial – Industrial – Military	 4.75 V to 5.25 V 4.75 V to 5.25 V 4.50 V to 5.50 V
Operating Ambient Temperature, T_A – Commercial – Industrial – Military	 0 to + 70°C – 40 to + 85°C – 55 to + 125°C

DC ELECTRICAL CHARACTERISTICS Across Temperature Range (Note 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
TTL INTERFACE							
V_{IL}	Low Level Input Voltage				0.8	V	2,3
V_{IH}	High Level Input Voltage		2.0			V	2,3
V_{OL}	Low Level Output Voltage	I_{OL} = Rated buffer current		0.2	0.4	V	2,3,4
V_{OH}	High Level Output Voltage	I_{OH} = Rated buffer current	2.4	3.4		V	2,3,4
V_{T+}	Schmitt Trig. +ve Threshold			2.0	2.4	V	
V_{T-}	Schmitt Trig. –ve. Threshold		0.6	0.8		V	
CMOS INTERFACE							
V_{IL}	Low Level Input Voltage				1.5	V	3
V_{IH}	High Level Input Voltage		3.5			V	3
V_{OL}	Low Level Output Voltage	I_O =Rated buffer current			0.4	V	3,5,6
V_{OH}	High Level Output Voltage	I_O =Rated buffer current	V_{DD}–0.5			V	3,5,7
V_{T+}	Schmitt Trig. +ve Threshold			3.0	4.0	V	
V_{T-}	Schmitt Trig. –ve Threshold		1.0	1.5		V	
GENERAL							
I_{IL}	Low Level Input Current	$V_I = V_{SS}$			+1	µA	
I_{IH}	High Level Input Current	$V_I = V_{DD}$			–1	µA	
I_{OZ}	Tri-state Output Leakage	V_O = 0 V or V_{DD}			± 10	µA	
C_{IN}	Input Capacitance	Freq = 1 MHz @ 0 V		2	4	pF	8
C_O	Output Capacitance	Freq = 1 MHz @ 0 V		4		pF	8
$C_{I/O}$	Bidi. I/O Capacitance	Freq = 1 MHz @ 0 V		4	8	pF	8
I_{KLU}	I/O Latch-up Current	$V < V_{SS}$, $V > V_{DD}$	500			mA	
V_{ESD}	Electrostatic Protection	C=100 pF, R =1.5 KΩ	4000			V	
PD_G	Power Dissipation per gate			6		µW/Gate/MHz	9
PD_O	Power Dissipation per Output	C = 50 pF		1.5		mW/Output/MHz	9

Notes 1. Commercial 0 to 70°C, V_{DD} = 5 V ± 5%.
Industrial –40 to 85°C, V_{DD} = 5 V ± 5%.
Military –55 to 125 °C, V_{DD} = 5 V ± 10%.
2. Adherence to rules in Power Requirements section required.
3. Refer to the Design Manual for AC Testing Levels and Conditions
4. Buffers offered in 3, 6, 12, 16, 24, 48 mA TTL options. The 48mA buffer is rated for sink current only.
5. Buffers are available in 2, 4 and 8mA CMOS options.

AC ELECTRICAL CHARACTERISTICS V_{DD} = 5 V, T_A = 25°C (Note)

Internal Macrocells					Propagation Delays (ns) Standard Loads (1)		
Cell Name	Symbol	Area (μm^2)			4	16	32
Inverter	IV	285	A to Z	t_{PHL}	0.33	0.75	1.32
				t_{PLH}	0.33	0.79	1.40
D Flip-Flop, double drive	FD1P	2709	CP to Q	t_{PHL}	0.99	1.22	1.53
				t_{PLH}	0.93	0.16	1.48
			CP to QN	t_{PHL}	1.21	1.43	1.69
				t_{PLH}	1.16	1.38	1.73
			D	t_S	0.38		
				t_H	–		
			CP	t_{PWL}	0.95		
				t_{PWH}	1.14		
D Flip-Flop, double buffered outputs	FD2S	3421	CP to Q	t_{PHL}	1.05	1.54	2.20
				t_{PLH}	0.91	1.36	1.96
			CP to QN	t_{PHL}	1.12	1.58	2.19
				t_{PLH}	1.11	1.47	1.94
			D	t_S	0.62		
				t_H	–		
			CP	t_{PWL}	0.92		
				t_{PWH}	0.92		
D Latch, double buffered outputs	LD3P	1996	CD to Q	t_{PHL}	0.58	0.81	1.12
				t_{PLH}	–	–	–
			CD to QN	t_{PHL}	–	–	–
				t_{PLH}	0.77	1.98	1.27
			D	t_S	0.79		
				t_H	0.18		
			CD	t_{PWL}	0.62		
				t_{PWH}	–		
2-Input NAND double drive	ND2P	570	A to Z	t_{PHL}	0.28	0.67	1.20
				t_{PLH}	0.37	0.81	1.40

AC ELECTRICAL CHARACTERISTICS V_{DD} = 5 V, T_A = 25°C (Note)

External Macrocells				Propagation Delays (ns) Standard Loads (1)		
Input Interface						
Cell Name	**Symbol**			**4**	**16**	**64**
TTL Input Buffer	TLCHT	A to Z	t_{PHL}	0.61	0.69	0.96
			t_{PLH}	0.43	0.49	0.71
TTL Schmitt Trigger Input Buffer	SCHMITT	A to Z	t_{PHL}	0.81	0.94	1.36
			t_{PLH}	0.90	0.97	1.20
CMOS Input Buffer	IBUF	A to Z	t_{PHL}	0.47	0.55	0.84
			t_{PLH}	0.54	0.62	0.83
CMOS Schmitt Trigger Input Buffer	SCHMITC	A to Z	t_{PHL}	0.79	0.91	1.24
			t_{PLH}	1.78	1.86	2.15
Outputs				**Output Load Capacitance**		
Cell Name	**Symbol**			**50pF**	**85pF**	**250pF**
TTL Bus Driver Output Buffer (12 mA, Slew Rate Control)	BU12R	A to Z	t_{PHL}	3.47	4.36	8.55
			t_{PLH}	2.91	3.26	4.91
				50pF	**250pF**	**500pF**
TTL Tristate Bus Driver Output Buffer (18 mA, Slew Rate Control)	BUT18R	A to Z	t_{PHL}	3.64	7.10	11.43
			t_{PLH}	2.94	4.68	6.85
				50pF	**300pF**	**600pF**
Bidirectional TTL Buffer Tristate Bus Driver Output (24mA, Slew Rate Control)	BUD24STR	A to IO	t_{PHL}	3.66	7.49	11.96
			t_{PLH}	3.04	4.94	7.22

Note: 1. Please refer to the CB22000 Design Manual for standard load equivalents for estimated wirelengths.

APPENDIX - MACROCELL LIBRARY

Cell	Description	Area (μm^2)
AND FUNCTIONS		
AN2	2 Input AND, Single Drive	570
AN2P	2 Input AND, Double Drive	713
AN3	3 Input AND, Single Drive	713
AN3P	3 Input AND, Double Drive	855
AN4	4 Input AND, Single Drive	855
AN4P	4 Input AND, Double Drive	998
NAND FUNCTIONS		
ND2	2 Input NAND, Single Drive	428
ND2P	2 Input NAND, Double Drive	570
ND3	3 Input NAND, Single Drive	570
ND3P	3 Input NAND, Double Drive	1140
ND4	4 Input NAND, Single Drive	713
ND4P	4 Input NAND, Double Drive	1283
ND5	5 Input NAND, Single Drive	1140
ND5P	5 Input NAND, Double Drive	1568
ND6	6 Input NAND, Single Drive	1426
ND6P	6 Input NAND, Double Drive	1568
ND8	8 Input NAND, Single Drive	1711
ND8P	8 Input NAND, Double Drive	1853
NOR FUNCTIONS		
NR2	2 Input NOR, Single Drive	428
NR2P	2 Input NOR, Double Drive	713
NR3	3 Input NOR, Single Drive	570
NR3P	3 Input NOR, Double Drive	1140
NR4	4 Input NOR, Single Drive	713
NR4P	4 Input NOR, Double Drive	1283
NR5	5 Input NOR, Single Drive	855
NR5P	5 Input NOR, Double Drive	1426
NR6	6 Input NOR, Single Drive	1568
NR6P	6 Input NOR, Double Drive	1711
NR8	8 Input NOR, Single Drive	1711
NR8P	8 Input NOR, Double Drive	1853
OR FUNCTIONS		
OR2	2 Input OR, Single Drive	570
OR2P	2 Input OR, Double Drive	713
OR3	3 Input OR, Single Drive	713
OR3P	3 Input OR, Double Drive	713
OR4	4 Input OR, Single Drive	855
OR4P	4 Input OR, Double Drive	998

Cell	Description	Area (μm^2)
AND-NOR FUNCTIONS		
AO1	2 Input AND into 3 Input NOR, $\overline{(AB+C+D)}$	713
AO2	Double 2 Input AND into 2 Input NOR, $\overline{(AB+CD)}$	713
AO2P	Double 2 Input AND into 2 Input NOR, Double Drive, (AB+CD)	1283
AO5	Inverting 2 of 3 Majority Gate, $\overline{(AB+AC+BC)}$	998
AO6	2 Input AND into 2 Input NOR, $\overline{(AB+C)}$	4570
EO1	2 Input AND + 2 Input NOR into 2 Input NOR, $\overline{(AB+not(C+D))}$	855
OR-NAND FUNCTIONS		
AO3	2 Input OR into 3 Input NAND, $\overline{((A+B)CD)}$	713
AO3P	2 Input OR into 3 Input NAND, Double Drive, $\overline{((A+B)CD)}$	1426
AO4	Double 2 Input OR into 2 Input NAND, $\overline{((A+B)(C+D))}$	713
AO7	2 Input OR into 2 Input NAND, $\overline{((A+B)C)}$	570
EON1	2 Input OR + 2 Input NAND into 2-Input NAND, $\overline{((A+B).not(CD))}$	998
EON1P	2 Input OR + 2 Input NAND into 2 Input NAND, Double Drive, $\overline{((A+B).not(CD))}$	1426
ADDER FUNCTIONS		
FA1A	Full Adder	2851
INVERTER FUNCTIONS		
B1A	Inverter, 12x(Z)	1853
B2A	Inverter, 24x(Z)	3564
B4I	Inverter, 4x(Z)	713
B4IP	Inverter, 8x(Z)	1283
B5I	Inverter, 3x(Z)	570
B5IP	Inverter, 6x(Z)	998
IV	Inverter, 1x(Z)	285
IVA	Inverter, Double P Transistor, Single N Transistor	428
IVD	2x Drive Uncommitted Inverter Pair	570
IVP	Inverter, 2x(Z)	428
DUAL INVERTER FUNCTIONS		
B2I	Dual Inverters, 1x(Z1), 3x(Z2)	855
B2IP	Dual Inverters, 2x(Z1), 6x(Z2)	1283
B3I	Dual Inverters, 2x(Z1), 2x(Z2)	713
B3IP	Dual Inverters, 4x(Z1), 4x(Z2)	1283
IVDA	Dual Inverters, 1x(Y), 1x(Z)	570
IVDAP	Dual Inverters, 2x(Y), 2x(Z)	855
NON-INVERTING BUFFER FUNCTIONS		
BTREE	Internal Non-Inverting Buffer, Single In Phase Output	1426

Cell	Description	Area (μm^2)
EXCLUSIVE OR/NOR FUNCTIONS		
EN	2 Input Exclusive NOR, Single Drive	998
EN3	3 Input Exclusive NOR, Single Drive	1996
EN3P	3 Input Exclusive NOR, Double Drive	1996
ENP	2 Input Exclusive NOR, Double Drive	1426
EO	2 Input Exclusive OR, Single Drive	855
EO3	3 Input Exclusive OR, Single Drive	1853
EO3P	3 Input Exclusive OR, Double Drive	996
EOP	2 Input Exclusive OR, Double Drive	1426
INTERNAL TRISTATE FUNCTIONS		
BTS4	Internal Tristate Buffer, Positive Enable, Single Drive	713
BTS4P	Internal Tristate Buffer, Positive Enable, Double Drive	998
BTS5	Internal Tristate Inverting Buffer, Positive Enable, Single Drive	570
BTS5P	Internal Tristate Inverting Buffer, Positive Enable, Double Drive	998
CMOS INPUT BUFFERS		
IBUF	CMOS Input Buffer	99364
IBUFD	CMOS Input Buffer with Active Pull-Down	99364
IBUFN	Inverting CMOS Input Buffer	100077
IBUFU	CMOS Input Buffer with Active Pull-Up	99364
SCHMITT INPUT BUFFERS		
SCHMITC	CMOS Schmitt Trigger Input Buffer	99364
SCHMITCD	CMOS Schmitt Trigger Input Buffer, Active Pull-Down	99364
SCHMITCN	Inverting CMOS Schmitt Trigger Input Buffer	100077
SCHMITCU	CMOS Schmitt Trigger Input Buffer, Active Pull-Up	99364
SCHMITT	TTL Schmitt Trigger Input Buffer	99364
SCHMITTD	TTL Schmitt Trigger Input Buffer, Active Pull-Down	99364
SCHMITTN	Inverting TTL Schmitt Trigger Input Buffer	100077
SCHMITTU	TTL Schmitt Trigger Input Buffer, Active Pull-Up	99364
TTL INPUT BUFFERS		
TLCHT	TTL Input Buffer	99364
TLCHTD	TTL Input Buffer, Active Pull-Down	99364
TLCHTN	Inverting TTL Input Buffer	100077
TLCHTU	TTL Input Buffer, Active Pull-Up	99364
D FLIP-FLOP FUNCTIONS		
FD1	D Flip-Flop, Buffered Outputs	2424
FD11S	D Flip-Flop, with Scan Input, Buffered Outputs	3849
FD12S	D Flip-Flop, with Double Scan Input, Buffered Outputs	4847
FD1P	D Flip-Flop, Double Buffered Outputs	2709
FD1S	D Flip-Flop with Scan Input, Buffered Outputs	3136

Cell	Description	Area (μm^2)
FD2	D Flip-Flop with Clear, Buffered Outputs	2566
FD22S	D Flip-Flop with Double Scan Input with Clear, Buffered Outputs	4847
FD2P	D Flip-Flop with Clear, Double Buffered Outputs	4847
FD2S	D Flip-Flop with Scan Input with Clear, Buffered Outputs	3421
FD2TS	D Flip-Flop with Added Tristate Ouput	2994
FD3	D Flip-Flop with Clear and Preset, Buffered Outputs	2709
FD3P	D Flip-Flop with Clear and Preset, Double Buffered Outputs	2994
FD3S	D Flip-Flop with Scan Input, Clear and Preset, Buffered Outputs	3564
FD4	D Flip-Flop with Preset, Buffered Outputs	2709
FD42S	D Flip-Flop with Double Scan Input, Set Direct, Buffered Outputs	4704
FD4P	D Flip-Flop with Preset, Double Buffered Outputs	2994
FD4S	D Flip-Flop with Scan Input, Preset, Buffered Outputs	3564

J K FLIP-FLOP FUNCTIONS

FJK1	JK Flip-Flop, Buffered Outputs	3279
FJK1P	JK Flip-Flop, Double Buffered Outputs	3564
FJK1S	JK Flip-Flop with Scan Input, Buffered Output	4134
FJK2	JK Flip-Flop with Clear, Buffered Outputs	3421
FJK2P	JK Flip-Flop with Clear, Double Buffered Outputs	3707
FJK2S	JK Flip-Flop with Scan Input, Clear, Buffered Outputs	4277
FJK3	JK Flip-Flop with Clear and Preset, Buffered Outputs	3564
FJK3P	JK Flip-Flop with Clear and Preset, Double Buffered Output	3849
FJK3S	JK Flip-Flop with Scan Input, Clear and Preset, Buffered Outputs	4419

LATCH FUNCTIONS

LD1	D-Latch, Active High Clock, Buffered Outputs	1568
LD1P	D-Latch, Active High Clock, Double Buffered Outputs	1853
LD2	D-Latch, Active Low Clock, Buffered Outputs	1568
LD2P	D-Latch, Active Low Clock, Double Buffered Outputs	1853
LD3	D-Latch, Active High Clock, Active Low Clear, Buffered Outputs	1711
LD3P	D-Latch, Active High Clock, Active Low Clear, Double Buffered Outputs	1996
LD4	D-Latch, Active Low Clock, Active Low Clear, Buffered Outputs	1711
LD4P	D-Latch, Active Low Clock, Active Low Clear, Double Buffered Outputs	1996
LS1	D-Latch with Scan Test Inputs, Dual Active High Clocks, Buffered Outputs	2566
LS2	LS1 D-Latch into LD1 D-Latch, Active High Clocks, Buffered Outputs	4134
LSR1	SR Latch with Clear/Set, Separate Inputs, (Cross Coupled AO3 Macros)	1568
LSR2	SR Latch with Clear/Set, Common Gated Inputs, (Cross Coupled AO3 Macros)	1568
RAM1	Gated D-Latch with Added Tristate Output	1568

Cell	Description	Area (μm^2)
MULTIPLEXER FUNCTIONS		
MUX21L	2:1 Multiplexer, 1 Phase Select, Unbuffered Inputs, Inverting Buffered Output	998
MUX21LA	2:1 Multiplexer, 2 Phase Select, Unbuffered Inputs, Inverting Buffered Output	998
MUX21LB	2:1 Non-Inverting Multiplexer, 2 Phase Select, Unbuffered Inputs, Inverting Buffered Output	1140
MUX21LP	2:1 Multiplexer, 1 Phase Select, Unbuffered Inputs, Inverting Double Buffered Output	1140
MUX41	4:1 Multiplexer, Buffered Inputs, 2 Select Lines, Buffered Output	2281
MUX41L	4:1 Multiplexer, Buffered Inputs, 2 Select Lines, Inverting Buffered Output	2424
MUX41P	4:1 Multiplexer, Buffered Inputs, 2 Select Lines, Double Drive Buffered Output	2424
MUX81	8:1 Multiplexer, Buffered Inputs, 3 Select Lines, Buffered Output	4990
MUX81H	8:1 Multiplexer, Buffered Inputs, 3 Select Lines, Buffered Output	4990
MUX81P	8:1 Multiplexer, Buffered Inputs, 3 Select Lines, Double Buffered Output	5132

Cell	Description	Standard Units
CMOS OUTPUT BUFFER		
B2CR	CMOS Output Buffer, 2mA, Slew Rate Control	1
B4CR	CMOS Output Buffer, 4mA, Slew Rate Control	2
B8CR	CMOS Output Buffer, 8mA, Slew Rate Control	4
TTL OUTPUT BUFFERS		
B2R	TTL Output Buffer, 2mA, with Slew Rate Control	2
B4	TTL Output Buffer, 4mA	8
B4R	TTL Output Buffer, 4mA, with Slew Rate Control	4
B4ROD	TTL Open Drain Output Buffer, 4mA, with Slew Rate Control	4
B8	TTL Output Buffer, 8mA	16
B8R	TTL Output Buffer, 8mA, with Slew Rate Control	8
B8ROD	TTL Open Drain Output Buffer, 8mA, with Slew Rate Control	8
CMOS BIDIRECTIONAL BUFFER		
BD2C	Bidirectional CMOS I/O Buffer, 2mA	2
BD2CR	Bidirectional CMOS I/O Buffer, 2mA, with Slew Rate Control	1
BD2CRU	Bidirectional CMOS I/O Buffer, Active Pull Up, 2mA, Slew Rate Control	1
BD2SCR	Bidirectional CMOS I/O Buffer, Schmitt trigger Input, 2mA, Slew Rate Control	1
BD2SCRU	Bidirectional CMOS I/O Buffer, Schmitt trigger Input, Active Pull Up, 2mA, with Slew Rate Control	1
BD4C	Bidirectional CMOS I/O Buffer, 4mA	4
BD4CR	Bidirectional CMOS I/O Buffer, 4mA, with Slew Rate Control	2
BD4CRU	Bidirectional CMOS I/O Buffer, Active Pull Up, 4mA, with Slew Rate Control	2
BD4SCR	Bidirectional CMOS I/O Buffer, Schmitt Trigger Input, 4mA, with Slew Rate Control	2
BD4SCROD	Bidirectional CMOS I/O Buffer, Schmitt Trigger Input, Open Drain Output, 4mA, with Slew Rate Control	2
BD4SCRU	Bidirectional CMOS I/O Buffer, Active Pull Up, Schmitt Trigger Input, 4mA, Slew Rate Control	2
BD8SCR	Bidirectional CMOS I/O Buffer, Schmitt Trigger Input, 8mA, Slew Rate Control	4
BD8SCRU	Bidirectional CMOS I/O Buffer, Active Pull Up, Schmitt Trigger Input, 8mA, Slew Rate Control	4
TTL BIDIRECTIONAL BUFFERS		
BD2STR	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, 2 mA, with Slew Rate Control	2
BD2STRU	Bidirectional TTL I/O Buffer, Active pull Up, Schmitt Trigger Input, 2 mA, with Slew Rate Control	2
BD2TR	Bidirectional TTL I/O Buffer, 2 mA, with Slew Rate Control	2
BD2TRU	Bidirectional TTL I/O Buffer, Active Pull Up,with Slew Rate Control	2
BD4STR	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, 4mA, with Slew Rate Control	4

Cell	Description	Standard Units
BD4STROD	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, Open Drain Output, 4mA, with Slew Rate Control	4
BD4STRU	Bidirectional TTL I/O Buffer, Active Pull-Up, Schmitt Trigger Input, 4mA, with Slew Rate Control	4
BD4T	Bidirectional TTL I/O Buffer, 4mA	8
BD4TR	Bidirectional TTL I/O Buffer, 4mA, with Slew Rate Control	4
BD4TRU	Bidirectional TTL I/O Buffer, Active Pull-Up, 4mA, with Slew Rate Control	4
BD8STR	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, 8mA, with Slew Rate Control	8
BD8STRD	Bidirectional TTL I/O Buffer, Active Pull Down, Schmitt Trigger Input, 8mA, with Slew Rate Control	8
BD8STROD	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, Open drain Output, 8mA, with Slew Rate Control	8
BD8STRU	Bidirectional TTL I/O Buffer, Active Pull-Up, Schmitt Trigger Input, 8mA, with Slew Rate Control	8

CMOS TRISTATE OUTPUT BUFFERS

BT2CR	CMOS Tristate Output Bufferm 2 mA with Slew Rate Control	1
BT2CRU	CMOS Tristate Output Buffer, Active Pull Up, 4mA with Slew Rate Control	1
BT4CR	CMOS Tristate Output Buffer, 4mA with Slew Rate Control	2
BT4CRU	CMOS Tristate Output Buffer, Active Pull-Up, 4mA, with Slew Rate Control	2
BT8CR	CMOS tristate Output Buffer, 8mA with Slew Rate Control	4
BT8CRU	CMOS Tristate Output Buffer, Active Pull Up, 8mA with Slew Rate Control	4

TTL TRISTATE OUTPUT BUFFERS

BT2R	TTL Tristate Output Buffer, 2mA, with Slew Rate Control	2
BT2RU	TTL Tristate Output Buffer, Active Pull-Up, 2mA, with Slew Rate Control	2
BT4	TTL Tristate Output Buffer, 4mA	8
BT4OD	TTL Tristate Open Drain Output Buffer, 4mA	8
BT4R	TTL Tristate Output Buffer, 4mA, with Slew Rate Control	4
BT4RU	TTL Tristate Output Buffer, Active Pull-Up, 4mA, with Slew Rate Control	4
BT8	TTL Tristate Output Buffer, 8mA	16
BT8OD	TTL Tristate Open Drain Output Buffer, 8mA	16
BT8R	TTL Tristate Output Buffer, 8mA, with Slew Rate Control	8
BT8RU	TTL Tristate Output Buffer, Active Pull-Up, 8mA, with Slew Rate Control	8

Cell	Description	Standard Units
TTL BUS DRIVER OUTPUT BUFFER		
BU6R	TTL Bus Driver Output Buffer, 6mA with Slew Rate Control	6
BU12R	TTL Bus Driver Output Buffer, 12mA with Slew Rate Control	12
BU18R	TTL Bus Driver Output Buffer, 18mA with Slew Rate Control	18
BU24R	TTL Bus Driver Output Buffer, 24mA with Slew Rate Control	24
TTL BIDIRECTIONAL BUFFER WITH TRISTATE BUS DRIVER OUTPUT		
BUD6STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 6mA, with Slew Rate Control	6
BUD6STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 6mA, (S = 5V)	12
BUD6STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 6mA, (S = 0V)	6
BUD12STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 12mA, with Slew Rate Control	12
BUD12STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 12mA, (S = 5V)	24
BUD12STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 12mA, (S = 0V)	12
BUD18STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 18mA, with Slew Rate Control	18
BUD18STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 18mA, (S = 5V)	36
BUD18STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 18mA, (S = 0V)	18
BUD24STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 24mA, with Slew Rate Control	24
BUD24STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 24mA, (S = 5V)	48
BUD24STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 24mA, (S = 0V)	24
TTL TRISTATE BUS DRIVER OUTPUT BUFFER		
BUT6R	TTL Tristate Bus Driver Output Buffer, 6mA with Slew Rate Control	6
BUT12R	TTL Tristate Bus Driver Output Buffer, 12mA with Slew Rate Control	12
BUT18R	TTL Tristate Bus Driver Output Buffer, 18mA with Slew Rate Control	18
BUT24R	TTL Tristate Bus Driver Output Buffer, 24mA with Slew Rate Control	24

NOTES: